IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

J. P. KOTOWSKI, ET AL.

Application No. 10/067,441

Filed: February 4, 2002

For: **INTEGRATED CIRCUIT AND METHOD FOR TESTING SAME USING SINGLE PIN TO CONTROL TEST MODE AND NORMAL MODE OPERATION**

Group Art Unit: 2824

Examiner: JUNG H. HUR

DECLARATION BY JEFFREY P. KOTOWSKI AND KYLE FODCHUK UNDER 37 CFR 1.131 TO OVERCOME CITED PATENT

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Attorney Docket: NSC1-G9800
[P05051]

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

1. This declaration is to establish completion of the invention in the above-referenced application (the '441 application) in the United States at a date prior to January 23, 2002. January 23, 2002 is the effective date of the published patent application cited by the Examiner and will be referred to in this declaration as the "Critical date."

2. We are the two inventors of the invention claimed in the '441 application (the "Invention").

3. The '441 application discloses: an integrated circuit having an external node (and typically also additional external nodes), operational circuitry configured to operate in response to at least one control signal determined by a signal asserted to the external node from an external source, and test circuitry coupled to the external node and the operational circuitry. The test circuitry is operable in a test mode in response to test data received at the external node from an external source, and is configured to assert to the operational circuitry a control signal in response to an external control signal received at the external node;

test circuitry for use in a circuit having an access node and operational circuitry that operates in response to a control signal determined by a signal asserted to the access node. The test circuitry includes logic circuitry configured to be coupled to the access node and the operational circuitry, and additional circuitry coupled to the logic circuitry and configured to operate in the test mode in response to test data received at the access node. The logic circuitry can extract test data from an amplitude-modulated input signal asserted to the access node when the logic circuitry is coupled to the access node, and can generate the control signal in response to the input signal and assert the control signal to the operational circuitry when the logic circuitry is coupled to the access node and the operational circuitry; and

a method for performing on-chip testing (or configuration or reconfiguration) and control of operational circuitry within an integrated circuit in response to test data and at least one control signal asserted from an external source to an external node of the integrated circuit.

4. All embodiments of the Invention were conceived in the United States before the Critical Date. This is apparent from the execution by declarant Kyle Fodchuk ("Mr. Fodchuk") on December 14, 2001, of the declaration filed with the '441 application. As evidenced by the text of that declaration, Mr. Fodchuk had, as of December 14, 2001, reviewed and understood the '441 application in the form in which it was filed on February 4, 2002.

5. We have assigned the Invention to National Semiconductor Corporation ("NSC"), as evidenced by the Assignment recorded in the U.S. Patent and Trademark Office at Reel 012573, Frame 0146, as of February 4, 2002. Mr. Fodchuk is an employee of NSC and was an employee of NSC during the year 2002.

6. During the period from January 14, 2002, through February 4, 2002, Mr. Fodchuk worked diligently and reasonably continuously toward reducing the Invention to practice.

7. During the year 2002, in the course of his duties for NSC, Mr. Fodchuk worked on the design of a low dropout ("LDO") voltage regulator integrated circuit that embodies the Invention, as evidenced by the attached declaration by Paul Werking (the "Werking" declaration) and the attachments to the Werking declaration.

8. During the year 2002, NSC manufactured and tested several prototypes of the LDO voltage regulator circuit. Two early integrated circuit prototypes of the LDO voltage regulator circuit embody the Invention, including a prototype known to NSC personnel as the "Hobbs 2" circuit, and a modified version of the Hobbs 2 circuit known to NSC personnel as the "Hobbs 3" circuit. The portion of the Hobbs 2 circuit that embodies the Invention is known to NSC personnel as the "OnePin circuit." The portion of the Hobbs 3 circuit that embodies the Invention is also known to NSC personnel as the "OnePin circuit."

9. During January 2002, including during January 8, 2002, through January 14, 2002, Mr. Fodchuk worked on the design of the Hobbs 2 circuit, including the design of its OnePin circuit, at NSC's facility in Grass Valley, California. Mr. Fodchuk attended a meeting on January 8, 2002 at NSC's facility in Grass Valley, California, at which the design of the Hobbs 2 circuit (including its OnePin circuit) was discussed by NSC personnel. On January 14, 2002, Mr. Fodchuk's engineering group at NSC submitted specifications for manufacturing the Hobbs 2 circuit to an NSC chip fabrication facility in Texas. On January 17, 2002, the layout for the Hobbs 2 circuit was placed on a reticle in accordance with the specifications submitted by Mr. Fodchuk's engineering group. Using this reticle (during January 18, 2002 to February 19, 2002), the Hobbs 2 circuit and other integrated circuits were manufactured at the NSC chip fabrication facility in Texas on each wafer of a wafer lot known within NSC as the "Saturn35" wafer lot. On each wafer of the Saturn35 wafer lot, the die that embodies the Hobbs 2 circuit is referred to by NSC as the "S35V20HA1" die.

10. Attached Exhibit A is a diagram of a wafer of the Saturn35 wafer lot, showing the die (labeled "S35V20HA1") that embodies the Hobbs 2 circuit and also showing other dies on the wafer. Attached Exhibit B is a listing of the dies on each wafer of the Saturn35 wafer lot.

11. During January 8, 2002, through February 4, 2002, Mr. Fodchuk worked diligently and reasonably continuously (at NSC's facility in Grass Valley, California) on the

design of the OnePin circuit of the Hobbs 2 circuit and the design of an improved version of the OnePin circuit of the Hobbs 2 circuit.

During January 14, 2002, through January 24, 2002 (including on January 24, 2002), Mr. Fodchuk designed modifications to the OnePin circuit of the Hobbs 2 chip, for implementation in the OnePin circuit of the Hobbs 3 chip (which was then being planned). Attached Exhibit C is a page dated January 24, 2002, from Mr. Fodchuk's laboratory notebook, which evidences this activity. Attached Exhibit D is another page from Mr. Fodchuk's laboratory notebook.

On February 1, 2002, Mr. Fodchuk designed and planned tests of the OnePin circuit of the Hobbs 2 chip and discussed the OnePin circuit (and plans to test it) with other NSC personnel. The portion of Exhibit D dated February 1, 2002 evidences this activity. The other portion of Exhibit D, dated February 5, 2002, lists additional modifications to the OnePin circuit of the Hobbs 2 chip (intended for implementation in the OnePin circuit of the Hobbs 3 chip) that were designed by Mr. Fodchuk at NSC's facility in Grass Valley, California, during January 24, 2002 through February 5, 2002.

On February 5, 2002, Mr. Fodchuk and other NSC personnel attended a meeting at NSC's facility in Grass Valley, California, at which Mr. Fodchuk presented and discussed changes to the OnePin circuit of the Hobbs 2 chip, which he proposed for implementation in the OnePin circuit of the Hobbs 3 chip.

12. The Hobbs 2 circuit is an integrated circuit, and includes an external node, operational circuitry, and test circuitry coupled to the external node and the operational circuitry. The test circuitry is configured to operate in a test mode in response to test data received at the external node from an external source. The test circuitry is also configured to assert to the operational circuitry a control signal in response to an external control signal received at the external node.

The test circuitry is configured to extract the test data from an amplitude-modulated input signal asserted to the external node from the external source, and to generate the control signal in response to the input signal. The external control signal is a binary signal determined by the input signal, and the test circuitry is operable in a mode in which the control signal is a binary signal whose state is determined by the state of the external control signal. The test circuitry is configured to extract a clock signal from the input signal, and to operate in response to the clock signal during the test mode.

The input signal has at least three levels, including a low level below a first threshold, a high level above a second threshold, and an intermediate level between the first threshold and the second threshold, and the test circuitry includes:

first comparator circuitry, coupled to receive the input signal and configured to operate in a first mode in which the first comparator circuitry generates a first signal indicative of whether the input signal has a level less than the first threshold; and

second comparator circuitry, coupled to receive the input signal and configured to operate in a first mode in which the second comparator circuitry generates a second signal indicative of whether the input signal has a level greater than the second threshold.

The test circuitry also includes a flip-flop having a set terminal, a reset terminal, and an output. The set terminal is coupled to receive the second signal, the reset terminal is coupled to receive the first signal, the output asserts a data signal in response to the first signal and the second signal, and the data signal is indicative of the test data.

The test circuitry includes comparator circuitry coupled and configured to receive the input signal, to extract the test data from the input signal, and to extract a latch signal from the input signal, and also includes at least one register coupled to the comparator circuitry for receiving the latch signal and at least some of the test data. The latch signal is indicative of whether the input signal had a level exceeding a latch threshold.

13. The Hobbs 2 circuit has an external node, and includes operational circuitry (configured to operate in response to at least one control signal) and test circuitry. During operation, the Hobbs 2 circuit is designed to control the operational circuitry and to perform at least one of testing, configuration, and reconfiguration of the operational circuitry, including by operating the test circuitry in a test mode in response to test data received at the external node from an external source, and asserting the at least one control signal from the test circuitry to the operational circuitry in response to an external control signal received at the external node.

14. The Hobbs 2 circuit includes an access node, operational circuitry (configured to operate in response to at least one control signal asserted to the access node), and test circuitry. The test circuitry includes logic circuitry configured to be coupled to the access node and to the operational circuitry; and additional circuitry coupled to the logic circuitry and configured to operate in a test mode in response to test data received at the access node.

The logic circuitry is configured to extract the test data from an amplitude-modulated input signal asserted to the access node when the logic circuitry is coupled to the access node, and to generate the control signal in response to the input signal and assert the control signal to the operational circuitry when the logic circuitry is coupled to the access node and to the operational circuitry.

The logic circuitry is configured to extract a clock signal from the input signal, and to assert the clock signal to the additional circuitry, when the logic circuitry is coupled to the access node and to the operational circuitry. The additional circuitry is configured to operate in response to the clock signal during the test mode.

The input signal has at least three levels, including a low level below a first threshold, a high level above a second threshold, and an intermediate level between the first threshold and the second threshold, and the logic circuitry includes:

first comparator circuitry, configured to be coupled to receive the input signal and to operate in a first mode in which said first comparator circuitry generates a first signal indicative of whether the input signal has a level less than the first threshold; and

second comparator circuitry, configured to be coupled to receive the input signal and to operate in a first mode in which said second comparator circuitry generates a second signal indicative of whether the input signal has a level greater than the second threshold.

The logic circuitry includes a flip-flop having a set terminal, a reset terminal, and an output. The reset terminal is coupled to receive the first signal, the set terminal is coupled to receive the second signal, the output asserted a data signal in response to the first signal and the second signal, and the data signal is indicative of the test data.

15. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that

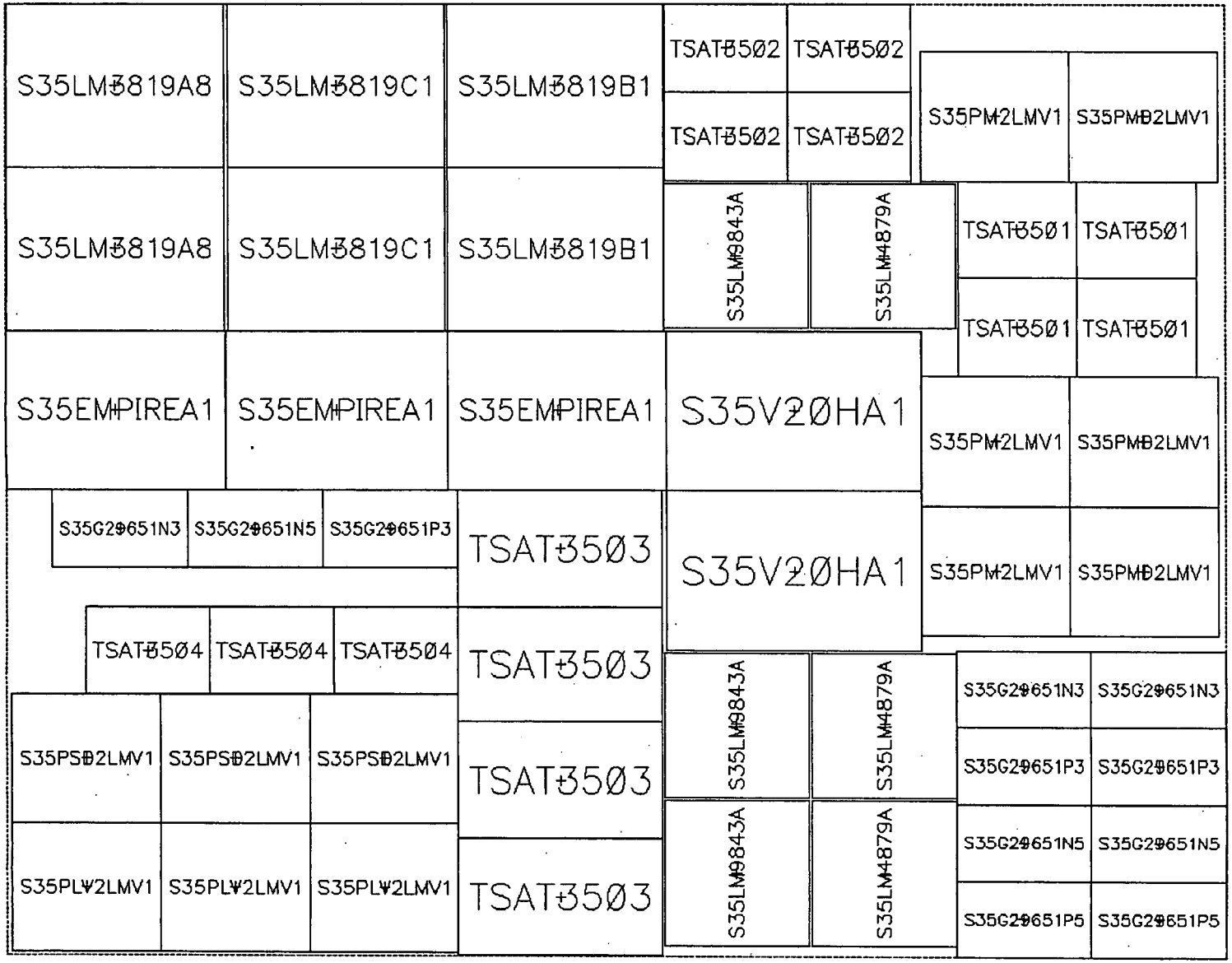
these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Executed on: _____ By: _____

JEFFREY P. KOTOWSKI

Executed on: June 10, 2003 By: _____

KYLE FODCHUK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S35LM5819B1
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TSAT5502
TSAT5502
TSAT5502
S35PM2LMV1
S35PMD2LMV1
S35LM5819A8
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S35LM5819B1
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S35LM4879A
TSAT5501
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TSAT5501
TSAT5501
S35EMPIREA1
S35EMPIREA1
S35EMPIREA1
S35V20HA1
S35PM2LMV1
S35PMD2LMV1
S35G29651N3
S35G29651N5
S35G29651P3
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S35V20HA1
S35PM2LMV1
S35PMD2LMV1
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TSAT5503
S35PSD2LMV1
S35PSD2LMV1
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S35LM9843A
S35LM4879A
S35G29651N3
S35G29651N3
S35G29651P3
S35G29651P3
S35PL¥2LMV1
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S35PL¥2LMV1
TSAT5503
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S35LM4879A
S35G29651N5
S35G29651N5
S35G29651P5
S35G29651P5

EXHIBIT A

SATURN35 DIESIZE

	DEVICE NAME	REQUESTOR	#	PHONE	XFW-/+	XFW-/+	SC	XSZ-/+	YSZ-/+	XFINAL	YFINAL	Proc.
1	S35PM2LMV1	S.CARPER	3	16395	991.0	859.0	0.72	713.16	618.12	1426.3	1236.2	sgvr2
2	S35PLV2LMV1	S.CARPER	3	16395	991.0	859.0	0.72	713.16	618.12	1426.3	1236.2	sgvr2
3	S35PSD2LMV1	S.CARPER	3	16395	991.0	859.0	0.72	713.16	618.12	1426.3	1236.2	sgvr2
4	S35PMD2LMV1	S.CARPER	3	16395	991.0	859.0	0.72	713.16	618.12	1426.3	1236.2	sgvr2
5	S35G29651P5	K.SCHOENDOERFER	2	82746556	899.0	511.0	0.72	646.92	367.56	1293.8	735.1	sg2
6	S35G29651N5	K.SCHOENDOERFER	3	82746556	899.0	511.0	0.72	646.92	367.56	1293.8	735.1	sg2
7	S35G29651N3	K.SCHOENDOERFER	3	82746556	899.0	511.0	0.72	646.92	367.56	1293.8	735.1	sg2
8	S35G29651P3	K.SCHOENDOERFER	3	82746556	899.0	511.0	0.72	646.92	367.56	1293.8	735.1	sg2
9	S35LM3819C1	K.SCHOENDOERFER	2	82746556	1446.0	1093.0	0.72	1040.76	786.60	2081.5	1573.2	sg3
10	S35LM3819B1	K.SCHOENDOERFER	2	82746556	1446.0	1093.0	0.72	1040.76	786.60	2081.5	1573.2	sg3
11	S35LM3819A8	K.SCHOENDOERFER	2	82746556	1446.0	1093.0	0.72	1040.76	786.60	2081.5	1573.2	sg3
12	S35EMPIREA1	M.NIGRO	3	82743076	1469.0	1060.0	0.72	1057.32	762.84	2114.6	1525.7	sg2
13	S35V20HA1	M.NIGRO	2	82743076	1704.0	1062.0	0.72	1226.52	764.28	2453.0	1528.6	sg2
14	S35LM9843A	R.SINGH	3	12738	968.0	968.0	0.72	696.60	696.60	1422.4	1422.4	sp2
15	S35LM4879A	R.SINGH	3	12738	968.0	968.0	0.72	696.60	696.60	1422.4	1422.4	sp2
16	TSAT3501	M.MERCER	4	87512382	797.0	656.0	0.72	573.48	471.96	1147.0	943.9	sg2
17	TSAT3502	R.MARKS	4	87512382	825.0	589.0	0.72	593.64	423.72	1187.3	847.4	sgvr3
18	TSAT3503	P.REYES	4	87512382	1367.0	774.0	0.72	983.88	556.92	1967.8	1113.8	sgvr3
19	TSAT3504	R.MARKS	3	87512382	825.0	589.0	0.72	593.64	423.72	1187.3	847.4	sgvr3

Note: process s2 = cs65s-2lm, sg2 = cs65sg-2lm, sg3 = cs65sg-3lm, sgvr2 = cs65sgvr-2lm, sgvr3= cs65sgvr-3lm
sp2 = cs65sp-2lm, sp3 = cs65sp-3lm. # = number of die on reticle.

EXHIBIT B

EXHIBIT C

Jan 24/02

problems with present ONEPIN:

- ~~when latch sig~~ if programmed, when the signal crosses Latch level the comparator to detect hi (3/4 rs EN) goes low when it should stay high.* Removed the problem *
- when cells are programmed, output of the EE cell is opposite to what we entered. We will fix this by including a buffer stage (2 inverters rather than the inverter that is in the cell now) → we will invert data going into EPROM
- removed inverter on Clock line of EEPROM cell. No need for delaying clock as previously suspected.
- changed test modes that enable EEPROM to be read back. When it is read back now it enters TMX<1> then after 2 clock cycles it enters TMX<6>. This outputs the data on EEPROM. Previously, the EEPROM was outputting only the last bit of EEPROM.

This is the revised

EXHIBIT D

Feb1

Spoke with Jerry Marshall, test engineer from Santa Clara, who shed some light on the advantages and disadvantages he foresees with the implementation of ONEPIN.

advantages: - able to remain in test mode ~~after~~ once tester has completed doing a task. No need to shut down and start again. What we do have to be careful of is if we are driving the line and that if the previous command was to readback, there is no excessive current feeding back into what's driving the output when it was being read. ~~With~~ Having the 5kΩ resistor present allows, at most, 1mA of current (V_{DD}=5V) over the line at any given time. Transistors can handle that.

requirements and specs of tester he would be using:

- C_{out} = 50 pF
- test time for each die 1-2s. Actual programming & trimming = 400 ms

Feb 5

- Changes made to ONEPIN
  - → increased W of the gate (changed ON resistance to 10K (40K prev))
  - → included analog readback circuitry (4 internal nodes, E^2 current readback)
  - → inverted data before entering E^2
  - → dedicated specific test mode to allow to write to E^2